REMARKS

Favorable reconsideration of this application, in light of the following discussion and in view of the present amendment, is respectfully requested.

Claims 1, 6, 14, 18 and 20 are amended. Claims 1, 2, 4 and 6-20 are pending.

I. Rejection under 35 U.S.C. § 103

In the Office Action, at page 2, claims 1, 6-8, 11, 12, 14, 15 and 17-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6, 446,213 to Yamaki in view of U.S. Patent No. 6, 336,161 to Watts. This rejection is respectfully traversed because the combination of the teachings of Yamaki and Watts does not suggest:

> a controller to enable a power saving standby mode, to control the power management controller to store an operating state stored in the system memory to the flash memory and to cut power supply to the system when the power saving standby mode is selected, the power saving standby mode being selected when a standby mode or a power saving mode is selected and the controller determines that the flash memory is connected to the system,

as recited in amended independent claim 1.

Further, the combination of the teachings of Yamaki and Watts does not suggest:

> selecting a power saving standby mode, the power saving standby mode being selected when a power saving mode or a standby mode is selected and a determination is made that a flash memory is connected to the system;
>
> storing an operating state stored in the system memory to the flash memory when the power saving standby mode is selected; and
>
> cutting power supply to the system after the operating state has been stored,

as recited in amended independent claim 6.

Also, the combination of the teachings of Yamaki and Watts does not suggest:

> a controller to control the power management controller to store an operating state data stored in the system memory to the flash memory when a power saving standby mode is selected, the power saving standby mode being selected when a standby mode or a power saving mode is selected and a determination is made that the flash memory is connected to the system, to cut the power supply to the system, and to store the operating state to the system memory when a normal mode is selected,

as recited in amended independent claim 14.

Additionally, the combination of the teachings of Yamaki and Watts does not suggest:

> copying an operating state data stored in the system memory to a flash memory when a power saving standby mode of the computer system is activated, the power saving standby mode being activated when a standby mode or a power saving mode is selected and a determination is made that the flash memory is connected to the system; and
>
> copying the operating state data back to the system memory when a normal mode of the computer system is activated,

as recited in amended independent claim 18.

Further, the combination of the teachings of Yamaki and Watts does not suggest:

> a basic input/output system of the computer system storing an operating state stored in the system memory to the flash memory and cutting power supply to the system, after being informed that the power saving standby mode is selected, the power saving standby mode being selected when a standby mode or a power saving mode is selected and a determination is made that the flash memory is connected to the system,

as recited in amended independent claim 20.

As a non-limiting example, the present invention according to claim 1, for example, is directed to a computer system including a system memory, a power management controller controlling a supply of power to the system, a flash memory and a controller. The controller enables a power saving standby mode and controls the power management controller to store an operating state stored in the system memory to the flash memory. The controller also cuts power supply to the system when the power saving standby mode is selected. The power saving standby mode is selected when a standby mode or a power saving mode is selected and the controller determines that the flash memory is connected to the system.

Yamaki discusses a software-based sleep control of an operating system in which, when a power supply switch of the system is turned off, devices of the system are set into a sleep mode in which there is no need to hold the preset hardware environment values, though the value preset for the main memory must be held. The hardware environment values are then saved in the main memory. As the system memory is a volatile memory, standby power needs to be continually supplied to save the hardware environment values stored in the system memory of Yamaki.

Yamaki does not discuss or suggest, however, that a power saving standby mode is enabled by the system. Yamaki discusses only a sleep state but does not distinguish between a standby mode and a power saving standby mode. Further, Yamaki does not discuss or suggest

that an operating state is stored to a memory when a power saving standby mode is selected, where the power saving standby mode is selected when a standby mode or a power saving mode is selected and the controller determines that a flash memory is connected to the system. In Yamaki, only a power standby mode, sleep state S3, is discussed. However, Yamaki does not distinguish between a power standby mode and a power saving standby mode.

In contrast, the present invention according to claim 1, for example, is directed to a system that controls a power management controller to store an operating state stored in a system memory to a flash memory and to cut power supply to the system when a power saving standby mode is selected. The power saving standby mode is selected when a standby mode or a power saving mode is selected and additionally a determination is made that a flash memory is connected to the system. Thus, the present invention of claim 1, for example, particularly clarifies that the power saving standby mode is only determined to be selected when either a standby mode or a power saving mode is selected and it is determined that a flash memory is connected to the system.

As more clearly shown in Fig. 3 and discussed at paragraphs 0048-50, for example, after the standby mode S31 is selected, a determination is made at S33 as to whether the flash memory is connected. If the flash memory is connected, then the operating state is stored in the flash memory and if the flash memory is not connected to the system, then at S34, the BIOS 17 conducts the procedure when the standby mode (or the maximum power saving mode) is selected in the computer system. Therefore, the power saving standby mode is only selected when a standby mode or a power saving mode is selected, and in addition, the flash memory is determined to be connected to the system.

Further, as conceded by the Examiner, Yamaki does not discuss or suggest that an operating state is stored from the system memory to the flash memory and a power supply is cut to the system when a power saving standby mode is selected. The Examiner indicates that Watts makes up for the deficiency in Yamaki. The Applicant respectfully disagrees.

Watts discusses only that after a power-down mode is initiated, hardware configuration information is stored in the flash EEPROM, and once all system information has been stored to the flash EEPROM or the hard drive, the computer is powered down. Watts does not discuss or suggest that an operating state is stored to the flash memory and power supply is cut to the system when a power saving standby mode is selected. As discussed above, a power-down mode is distinct from a power saving standby mode, in that as set forth in claim 1, for example, the power saving standby mode is determined to be selected when a standby mode or a power

saving mode is selected and additionally a determination is made that the flash memory is connected to the system. Watts discusses only that if a power-down mode is initiated then configuration information is stored from hardware devices into the flash EEPROM and then the system is powered down. Watts does not discuss or suggest that an operating state stored to the flash memory and the power supply is cut specifically when a power saving standby mode is selected. As discussed at paragraph 0050 of the present specification, the selection of the power saving standby mode corresponds with selecting a standby mode and determining that the flash memory is connected to the system.

In contrast, Watts only discusses that a power down mode is selected, and neither Yamaki nor Watts determines that a power saving standby mode is selected when a standby mode or a power saving mode is selected and a determination is made that the flash memory is connected to the system. Thus, according to the present invention of claim 1, for example, if a standby or a maximum power saving mode is selected and a flash memory is not connected to the system, the system conducts the procedure when a typical standby mode or maximum power saving mode is selected, but if the standby mode or the maximum power saving mode is selected and also the flash memory is determined to be connected to the system, then the system recognizes that a power saving standby mode is selected and stores an operating state to the flash memory and cuts power supply to the system based on the determination that the power saving standby mode has been selected.

Therefore, the combination of the teachings of Yamaki and Watts does not suggest, "a controller to enable a power saving standby mode, to control the power management controller to store an operating state stored in the system memory to the flash memory and to cut power supply to the system when the power saving standby mode is selected, the power saving standby mode being selected when a standby mode or a power saving mode is selected and the controller determines that the flash memory is connected to the system," as recited in amended independent claim 1. Additionally, the combination of the teachings of Yamaki and Watts does not suggest, "selecting a power saving standby mode, the power saving standby mode being selected when a power saving mode or a standby mode is selected and a determination is made that a flash memory is connected to the system; storing an operating state stored in the system memory to the flash memory when the power saving standby mode is selected; and cutting power supply to the system after the operating state has been stored," as recited in amended independent claim 6. Further, the combination of the teachings of Yamaki and Watts does not suggest, "a controller to control the power management controller to store an operating state data stored in the system memory to the flash memory when a power saving standby mode is

selected, the power saving standby mode being selected when a standby mode or a power saving mode is selected and a determination is made that the flash memory is connected to the system, to cut the power supply to the system, and to store the operating state to the system memory when a normal mode is selected," as recited in amended independent claim 14. Also, the combination of the teachings of Yamaki and Watts does not suggest, "copying an operating state data stored in the system memory to a flash memory when a power saving standby mode of the computer system is activated, the power saving standby mode being activated when a standby mode or a power saving mode is selected and a determination is made that the flash memory is connected to the system; and copying the operating state data back to the system memory when a normal mode of the computer system is activated," as recited in amended independent claim 18. The combination of the teachings of Yamaki and Watts additionally does not suggest, "a basic input/output system of the computer system storing an operating state stored in the system memory to the flash memory and cutting power supply to the system, after being informed that the power saving standby mode is selected, the power saving standby mode being selected when a standby mode or a power saving mode is selected and a determination is made that the flash memory is connected to the system," as recited in amended independent claim 20. Thus, claims 1, 6, 14, 18 and 20 patentably distinguish over the references relied upon for at the least the reasons notes above. Accordingly, withdrawal of the § 103(a) rejection is respectfully requested.

Claims 7, 8, 11, 12, 15, 17 and 19 depend either directly or indirectly from independent claims 1, 6, 14 and 18 and include all the features of their respective independent claims, plus additional features that are not discussed or suggested by the reference relied upon. For example, claim 12 recites that, "a predetermined time is set to enter the power saving standby mode." Therefore, claims 7, 8, 11, 12, 15, 17 and 19 patentably distinguish over the references relied upon for at least the reasons noted above. Accordingly, withdrawal of the § 103(a) rejection is respectfully requested.

In the Office Action, at page 5, claims 2, 9, 10, 13 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamaki in view of Watts, and further in view of U.S. Publication No. 2003/0145191 to Park. This rejection is respectfully traversed.

As discussed above with respect to independent claims 1, 6 and 14, the combination of the teachings of Yamaki and Watts does not suggest all the features of independent claims 1, 6 and 14. Park fails to make up for the deficiencies in Yamaki and Watts, specifically with respect to the selection of a power saving standby mode. Therefore, claims 1, 6 and 14 patentably

distinguish over the references relied upon. Claims 2, 9, 10, 13 and 16 depend from independent claims 1, 6 and 14 and include all the features of the respective independent claims, plus additional features that are not discussed or suggested by the references relied upon. For example, claim 13 recites that, "the controller controls the power management controller to copy the operating state stored in the flash memory to the system memory via the universal serial bus port when the power saving mode is changed to a normal mode." Therefore, claims 2, 9, 10, 13 and 16 patentably distinguish over the references relied upon for at least the reasons notes above. Accordingly, withdrawal of the § 103(a) rejection is respectfully requested.

Conclusion

In accordance with the foregoing, claims 1, 6, 14, 18 and 20 have been amended. Claims 1, 2, 4 and 6-20 are pending and under consideration.

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

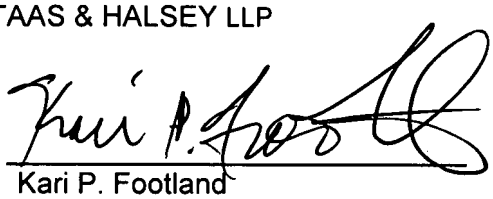
Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: August 30, 2007

By: 

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